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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,286	02/26/2002	Atsushi Takane	H6808.0004/P004	5346

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EXAMINER	
JOHNSTON, PHILLIP A	

ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·17

Office Action Summary	Application No.	Applicant(s)	
	10/082,286	TAKANE ET AL.	
	Examiner	Art Unit	
	Phillip A. Johnston	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This Office Action is submitted in response to RCE / Amendment filed 1-27-2005, wherein claims 1,24, and 25 have been amended. Claims 1-25 are pending.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-25 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of copending Application No. 10365383. Although the conflicting claims are not identical, they are not patentably distinct from each other because it is obvious to one of ordinary skill in the art that all the limitations in Claims 1-25 of Application No. 10082286 are contained in Claims 1-23 of Application No. 10365383. By way of example, a comparison of Claim 1 of Application No. 10082286, with Claims 15-18 of Application No. 10365383 is included below.

Claim 1, of Application No. 10082286, read as follows:

1. (Currently amended) A semiconductor inspection system, comprising:

a navigation system for storing design information such as CAD data of a

semiconductor chip and for setting capturing and inspecting conditions including a region on a semiconductor wafer subject to inspection based on the design information; and

a scanning electron microscope system for performing actual capturing of the semiconductor wafer and for executing inspection in accordance with the capturing and inspecting conditions being set,

wherein the navigation system sets a template comprising a bitmap based on the design information, and performs a matching process a pattern within a grayscale image provided by the scanning electron microscope, and wherein a portion of the image that corresponds to the template is re-registered as a new template in place of the bitmap based on the design information.

Claims 1,15, 17, and 18 of Application No. 10365383 read as follows;

1. A semiconductor inspection system, comprising: a navigation system for storing design information such as CAD data of a semiconductor chip and for setting capturing and inspecting conditions including a region on a semiconductor wafer subject to inspection based on the design information; and a scanning electron microscope system for performing actual capturing of the semiconductor wafer and for executing inspection in accordance with the capturing and inspecting conditions being set up.

15. The semiconductor inspection system according to claim 1, wherein the scanning electron microscope system comprises: means for generating an edge image by retrieving edge information from a scanning electron microscope image

obtained by capturing in the case of performing a matching process between the scanning electron microscope image and bitmap data from the design information as a template; means for re-registering a portion of the scanning electron microscope image as a template, said portion corresponding to a position of the edge image detected by the matching process between the edge image and design data; and means for using the re-registered template of the scanning electron microscope image in the subsequent matching process.

17. The semiconductor inspection system according to claim 15, wherein the scanning electron microscope system compares a correlation value between the design data and the scanning electron microscope image every time and re-registers a new template only when the compared correlation value is higher than the correlation value of the template used at that time.

18. The semiconductor inspection system according to claim 15, wherein the scanning electron microscope system performs an arbitrary frequency of the matching processes initially, the scanning electron microscope system compares correlation values between the design data and the scanning electron microscope images obtained in the arbitrary frequency of the matching processes, and the scanning electron microscope system re-registers the scanning electron microscope image having the highest correlation value as a new template.

It is obvious to one of ordinary skill in the art that all the limitations in Claims 1-25 of Application No. 10082286, are for the most part, contained in Claims 1-23 of Application No. 10365383. and anticipated by

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claims Rejection – 35 U.S.C. 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1,8,9,11-18,24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,363,167 to Miyano, in view of Ito, U.S. Patent No. 6,108,033.

Miyano (167) discloses the following;

(a) As shown in Figures 2 and 3, the recipe file 100 is selected according to a fine pattern in measurement, and read by the computer 101(St. 1). Then, a wafer (sample) 102 on which a photoresist pattern for forming an active area has been fabricated is transported into a specimen chamber of an SEM (an observation tool) (ST. 2). The wafer 102 is placed on a stage 103. Then rotation of the wafer 102 is corrected by an alignment operation (ST. 3). Then, the stage 103 is in a controlling manner moved to one of measurement areas recorded in the recipe file 100 by a stage controller 104 (ST. 4). Thereby, an observation field of an SEM is shifted onto a measurement area of the wafer 102. Then scanning an electron beam 105 is conducted across the measurement area and photoresist patterns present in the

measurement area are processed to an SEM image. In formation of the SEM image, focusing, magnification and the like are automatically adjusted (auto-focusing, ST. 5).

Then, the templates 11 to 13 are read into an image processor 106 (ST. 6). Thereafter, the SEM image obtained in ST. 5 (actual SEM image) is read into the image processor 106 and the actual SEM image is subjected to pattern matching with each of the templates 11 to 13, where correlation coefficients between the actual SEM image and a plurality of image templates are calculated and the coefficients are compared with one another to determine a matching point, as recited in claims 1,15, 24, and 25. See Column 4, line 40-67; Column 5, line 1-40; Figure 2 below;

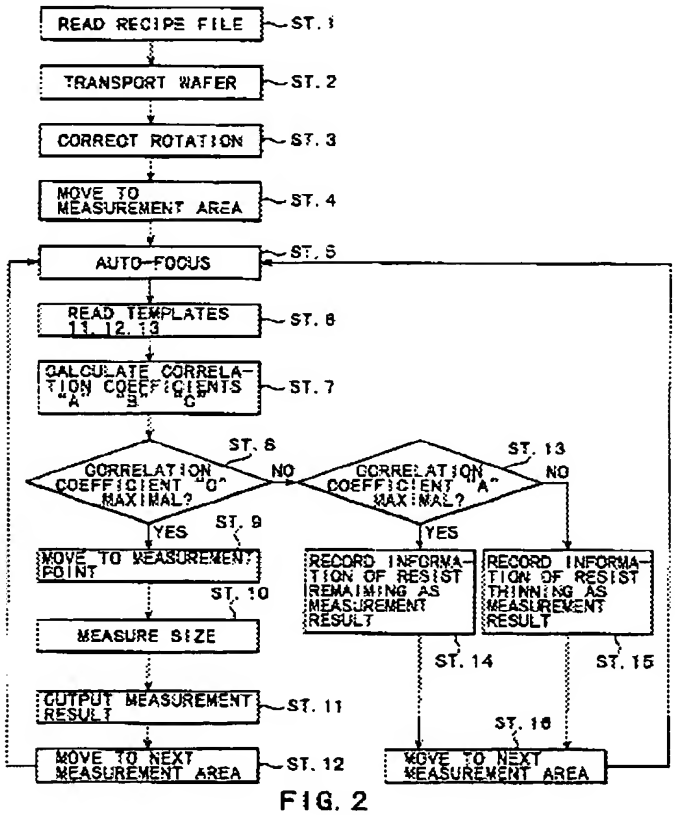


FIG. 2

(b) The templates 11 to 13 are made from images (SEM image) using a scanning electron microscope on patterns prepared actually or images obtained by lithography simulation from CAD data of photomasks (reticles). After templates 11 to 13 are read into an image processor 106 (ST. 6), the SEM image obtained in ST. 5 (actual SEM image) is read into the image processor 106 and the actual SEM image is subjected to pattern matching with each of the templates 11 to 13, and determining whether or not the correlation coefficient is maximal, as recited in claims 1,8,9,11,15,24,25,17 and 18. See Column 5, line 13-40; and Figures 1A-1C below;

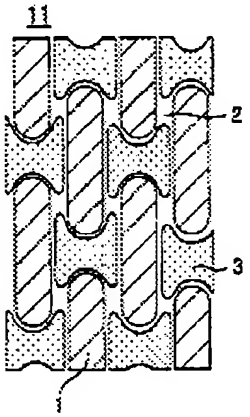


FIG. 1A

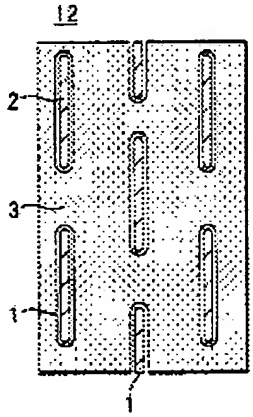


FIG. 1B

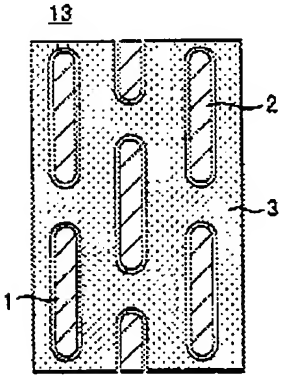


FIG. 1C

(c) In FIGS. 1A to 1C, a reference numeral 1 indicates a secondary electron image obtained from a photoresist pattern, a reference numeral 2 indicates a secondary electron image obtained from an edge of a photoresist pattern and a reference numeral 3 indicates a secondary electron image obtained from a part other than the photoresist patterns (a substrate), as recited in claims 11-15. See Column 4, line 33-40, and Figures 1A-1C above;

Miyano (167) as applied above fails to teach a scanning electron microscope image, wherein a portion of the image that corresponds to the template is re-registered as a new template in place of the bitmap based on the design information, as recited in claims 1,15,24, and 25. However, Ito (033) discloses an image processing apparatus and method where an object to be monitored picked up by an image pick-up unit, including a first step for producing a difference between an input image including a background image and an image of the object to be monitored from the image pick-up unit and the background image, as an image of the object; a second step for dividing the image of the object into a plurality of parts to produce a plurality of divided images of the object as a plurality of templates, a third step for matching each of a plurality of templates with a new input image and detecting a plurality of parts of the new input image having highest degrees of matching with the templates and a fourth step for updating the new templates using the parts of the new input image having the highest degrees of matching as a plurality of new templates. The fourth step is sequentially executed for new input images to sequentially update the templates to trace the object, as recited in claims 1,15,16,24, and 25. See Column 3, line 40-57.

Therefore it would have been obvious to one of ordinary skill in the art that the SEM measurement system and method of Miyano (167) can be modified to use the template registering method of Ito (033), to provide sequential updating of templates so that the stable matching is attained.

6. Claims 2-7,10 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyano (167) and Ito (033), in view of Lin, U.S. Patent No. 6,292,582.

Miyano (167) discloses the use of stored exposure and inspection conditions for executing the inspection judgement process; for example, in ST.13, when "being not maximal" is judged (NO), the photoresist pattern is most similar to the template 12. As a result, a failure of the photoresist pattern is classified into a group of "resist thinning." Thereafter, information of "resist thinning" is recorded as a measurement result. (ST. 15).

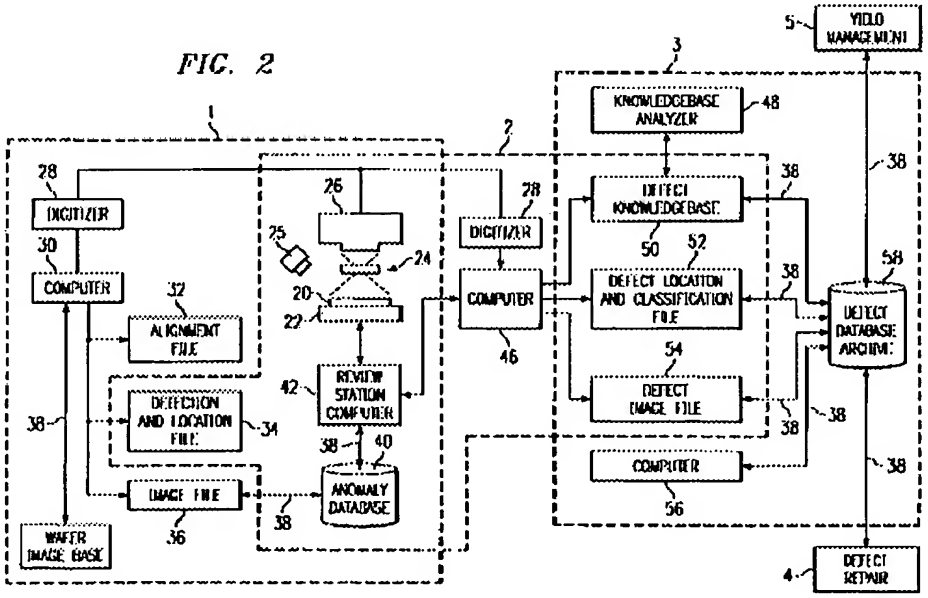
The information on failure obtained in ST.13 is presented on the wafer map of the display 107, for instance, as "no dimensional data" or in "a kind of failure" and a shot of non-resolution is visualized. Since the shot of non-resolution is visualized, discernment between resolution and non-resolution of a shot in exposure conditions for evaluation or a shape of the photoresist is clearly grasped at first glance. In addition, kinds of failures are automatically classified, as recited in claims 3-5,7, and 19-23. See Column 5, line 46-67; and Column 6, line 1-5.

The combination of Miyano (167) and Ito (033) fails to teach the use of an inspection system that includes a function to retrieve and store design data, as well as

transmitting data to other SEM systems via a network, as recited in claims 2-7, and 10. However, Lin (582) discloses;

(a) A defect detection and locating system in Figure 2, wherein a semiconductor wafer 20 is placed on an xy stage 22 so that an area of the wafer 20 is illuminated by an energy source 25 that produces energy such as white light, darkfield light, polarized light, laser refraction, scanning electrons, focused ion beams or X-ray such that anomalies on the wafer can be detected using a microscope 24 or other sensor device. A camera 26 or other image capturing device captures the microscope's 24 image while a digitizer 28, such as a frame grabber or other means of converting the image generated by the sensor from analog to digital form, supplies a digitized (bitmap) rendering of the image to an anomaly detecting-and-locating computer 30, as recited in claims 2-7, and 19-23. See Column 4, line 61-67; and Figure 2 below;

FIG. 2



(b) Yield management system 5, retrieves and analyzes information from the defect database/archive 58 and other information resources available on the network 38 and from other sources such as CAD Computer-Aided Designs, results of electrical tests carried out on wafers, wafer inspection reports and images, histories of defects, process models, wafer process histories, and packaged die failure reports, as recited in claims 2,6, and10. See Column 8, line 2-19.

(c) The architecture of the defect knowledgebase 50 allows for quick changes, fine tuning, regular maintenance, and optimization of the performance of the defect knowledgebase 50 that are desirable under production conditions due to changes in wafer processes, the need to provide more specific or more general classifications, changes in defect characteristics and frequency, and the emergence of new defects, as recited in claims19-23. See Column 30, line 27-65.

Therefore it would have been obvious to one of ordinary skill in the art that the measurement system of Miyano (167) and Ito (033) can be modified to use the resitive element forming method of Lin (582), to provide a method of storing, indexing and retrieving information, thereby providing rapid retrieval and access to the large amount of stored defect and image information so that files may be retrieved by other stations and systems connected to the network.

Conclusion

7. Any inquiry concerning this communication or earlier communications should be

directed to Phillip Johnston whose telephone number is (571) 272-2475. The examiner can normally be reached on Monday-Friday from 6:30 am to 3:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor John Lee can be reached at (571) 272-2477. The fax phone number for the organization where the application or proceeding is assigned is 703 872 9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PJ

April 15, 2005

JOHN R. LEE
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